Remarks

The Official Action rejected claims 1-9, 12-18, 22-24, 27-29 and 32-39. Applicant has amended claims 1, 2, 5, 8, 9, 12, 22, 24, 27 and 37 . Applicant respectfully requests allowance of the pending claims.

Information Disclosure Statement

The Official Action requested additional information regarding the numerous submitted prior art references. The submitted references include other applications of the Applicant having related disclosures. The submitted references also include numerous references supplied by foreign patent offices in regard to the present application and other applications of the Applicant.

Double Patenting/Terminal Disclaimer

The Official Action rejected claims 1-34 under the judicially created doctrine of obviousness-type double patenting. Applicant has elected to file a terminal disclaimer herewith in order to overcome the present rejection. Applicant respectfully requests the present rejection be withdrawn.

Claim Objections

The Official Action objected to claim 37 due to a typo. Applicant has amended claim 37 to correct the typo. Applicant respectfully requests the present objection be withdrawn.

Specification Objections

The Official Action objected to paragraph [0001]. Applicant has amended paragraph [0001] accordingly. Applicant respectfully requests the objection to paragraph [0001] be withdrawn.

Applicant further thanks the Examiner for pointing out the proper form for an Abstract. If the Examiner wishes to object to the Abstract, Applicant respectfully requests the Examiner to specific exactly in what regard the Abstract is being objected to. Applicant, however, believes the current Abstract complies with all ***requirements*** and respectfully points out that much of the cited language merely provides suggestions for Abstract content and not requirements for Abstract content.

Claim Rejections under 35 USC 112

The Official Action rejected claims 1-9, 12-18 and 22-24 under 35 USC 112, second paragraph, as being indefinite for failing to particular point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 8-9

Claims 8-9 were rejected for insufficient antecedent basis for the limitation "protected memory." Applicant has corrected claims 8-9 so they read "memory" instead of "protected memory" which finds antecedent basis in amended claim 1. Applicant respectfully requests withdrawal of the present rejection.

Claims 1-9, 12-18 and 22-24

Claims 1-9, 12-18 and 22-24 were rejected due to the limitation "private memory". In particular, the Official Action indicates that there is no definitive standard for ascertaining the scope of Applicant's claimed "private memory." While

Applicant believes the term "private memory" to be definite in light of the specification, Applicant has nonetheless amended claim 1 to more distinctly define the "memory" in claims 1-9, 12-18 and 22-23. Applicant respectfully points out that claim 24 did not and does not include the term "private memory". Withdrawal of the present rejection is earnestly solicited.

Claim Rejections Under 35 USC 102 (Davis)

The Official Action rejected claims 1, 6-9, 12-14, 16-18 and 22-24 under 35 USC 102(e) as being anticipated by Davis, US. Patent No. 6,401,208.

Claims 1, 6-9, 12-14, 16-18 and 22-23

Each of claims 1, 6-9, 12-14, 16-18 and 22-23 are directed to a processor comprising memory and one or more execution units. The one or more execution units authenticate an authenticated code module stored in the memory and execute the authenticated code module stored in the memory in response to executing a launch instruction. Further, claims 1, 6-9, 12-14, 16-18 and 22-23 requires that components separate from the processor are prevented from altering the authenticated code module stored in the memory.

The Official Action appears to rely on Davis which teaches a system that authenticates BIOS prior to BIOS execution. To this end, Davis appears to teach a processing unit 110 transferring bytes from a BIOS device to a cryptographic processor 170_1. (Davis at column 5, lines 55-65). Davis further teaches that the cryptographic processor 170_1 authenticates the bytes received from the BIOS device. (See, column 5, line 66 through column 6, line 13). Davis also teaches causing the processing unit 110 to execute BIOS code from the BIOS device upon the cryptographic processor 170_1 determining the BIOS code is authentic. (See,

column 5, lines 21-31). Accordingly, Davis appears to teach that the processing unit 110 executes the BIOS code from the BIOS device. However, claims 1, 6-9, 12-14, 16-18 and 22-23 require a processor to execute the authenticated code module from a memory that is part of the processor itself. Davis does not appear to teach that the BIOS device is part of the processing unit 110. In fact, Davis at column 1, lines 28-30 teaches the BIOS code is stored in a ROM device that is physically separate from the host processor (e.g. processing unit 110).

Since Davis does not appear to teach a processor that comprises a memory to store an authenticated code module and one or more execution units to execute the authenticated code module from the memory of the processor, Davis does not anticipate the invention of claims 1, 6-9, 12-14, 16-18 and 22-23. Applicant respectfully requests the rejection of claims 1, 6-9, 12-14, 16-18 and 22-23 be withdrawn.

Claim 24

Claim 24 is directed to a processor that comprises a memory, and one or more execution units to execute an authenticated code module stored in the memory. Accordingly, the above discussion regarding claims 1, 6-9, 12-14, 16-18 and 22-23 is relevant to the patentability of claim 24. Applicant respectfully requests the rejection of claim 24 be withdrawn.

Claim Rejections Under 35 USC 102 (McGarvey)

The Official Action rejected claims 1-5, 24 and 34-36 under 35 USC 102(b) as being anticipated by McGarvey, US. Patent No. 5,926,631.

Each of claims 1-5 and 24 are directed to ***a processor comprising memory and one or more execution units*** and claims 34-36 are directed to ***a processor***

comprising cache memory and one or more execution units. While the personal computer 300 of McGarvey likely contains a processor, McGarvey appears to provide no details regarding the processor of the personal computer 300. Accordingly, McGarvey does not teach a processor comprising memory/cache memory and execution units having the limitations of claims 1-5, 24 and 34-36.

The Official Action appears to rely on column 5, lines 46-57 of McGarvey for a teaching of the memory of claims 1-5 and 24 and the cache memory of claims 34-36. However, Applicant respectfully points out that the cited section describes web cache or network cache in which data retrieved via a network connection are stored to persistent storage such as a hard disk. (See, column 3, lines 10-11). In order to decrease the time for subsequent accesses to the same network data, the personal computer 300 can retrieve the network data from the hard disk instead of accessing the data again via the network. However, McGarvey appears to clearly teach that the cache is a hard disk or other type of persistent storage and not part of the processor as required by claims 1-5, 24 and 34-36. McGarvey therefore does not anticipate the invention of claims 1-5, 24 and 34-36. Applicant respectfully requests the present rejection of claims 1-5, 24 and 34-36 be withdrawn.

Claim Rejections Under 35 USC 102 (Sadovsky)

The Official Action rejected claims 1, 24 and 34 under 35 USC 102(b) as being anticipated by Sadovsky, US. Patent No. 5,689,638.

Each of claims 1 and 24 are directed to ***a processor comprising memory and one or more execution units*** and claim 34 is directed to ***a processor comprising cache memory and one or more execution units***. Sadovsky appears to teach a computer 22 having a processor or CPU 28 and a main memory 38. See,

Sadovsky at FIG. 1. Sadovsky further teaches a password cache 101 that is stored in the main memory 38. See, FIG. 4 and column 8, lines 11-23 of Sadovsky. Accordingly, the Official Action appears to be relying upon a cache that is not part of the processor as required by claims 1, 24 and 34. Applicant respectfully requests the present rejection of claims 1, 24 and 34 be withdrawn.

Claim Rejections Under 35 USC 102 (Peters)

The Official Action rejected claims 1, 24 and 34 under 35 USC 102(b) as being anticipated by Peters, US. Patent No. 6,393,420.

Each of claims 1 and 24 are directed to ***a processor comprising memory and one or more execution units*** and claim 34 is directed to ***a processor comprising cache memory and one or more execution units***. The Official Action appears to be relying on the validation cache of Peters for a teaching of the memory/cache memory of the processors of claims 1, 24 and 34. Peters describes what information is stored in the validation cache as well as the role of the validation cache. However, Applicant has been unable to locate where Peters describes how the validation cache is implemented. In particular, Applicant has been unable to locate anything in Peters to suggest that the validation cache is part of Peters' processor 12 as required by Applicant's claims 1, 24 and 34. In fact, given the nature of the validation cache, the validation cache is likely implemented as a file or some other structure stored on the storage 30. Since Peters does not appear to teach a processor comprising a memory and one or more execution units that having the other claimed limitations of claims 1, 24 and 34, Applicant respectfully requests the present rejection of claims 1, 24 and 34 be withdrawn.

Claim Rejections Under 35 USC 102 (Kedem)

The Official Action rejected claims 1, 24 and 34 under 35 USC 102(e) as being anticipated by Kedem, US. Patent No. 6,389,511.

Each of claims 1 and 24 are directed to ***a processor comprising memory and one or more execution units*** and claim 34 is directed to ***a processor comprising cache memory and one or more execution units***. The Official Action appears to be relying on the cache 44 of Kedem for a teaching of the memory/cache memory of the processors of claims 1, 24 and 34. However, the cache 44 is part of a storage subsystem 40 that may be connected to a host computer (not shown). See, Kedem at column 9, lines 24-26. Further, Kedem teaches that the cache 44 may be implemented with random access memory. Applicant has been unable to located any mention in Kedem of implementing the cache 44 as part of a processor. Since Kedem does not appear to teach a processor comprising a memory and one or more execution units that having the other claimed limitations of claims 1, 24 and 34, Applicant respectfully requests the present rejection of claims 1, 24 and 34 be withdrawn.

Claim Rejections Under 35 USC 103 (McGarvey/Schneier)

The Official Action rejected claim 37 under 35 USC 103(a) as being unpatentable over McGarvey in view of Schneier. Claim 37 includes claim 34 as a base claim and is therefore allowable for at least the reasons mentioned above. Withdrawal of the present rejection is respectfully requested.

Claim Rejections Under 35 USC 103 (McGarvey/Schneier/Abgrall)

The Official Action rejected claim 15 under 35 USC 103(a) as being unpatentable over McGarvey in view of Schneier in further view of Abgrall. Claim 15

includes claim 1 as a base claim and is therefore allowable for at least the reasons mentioned above. Withdrawal of the present rejection is respectfully requested.

Claim Rejections Under 35 USC 103 (McGarvey)

The Official Action rejected claims 38-39 under 35 USC 103(a) as being unpatentable over McGarvey. Claims 38-39 includes claim 34 as a base claim and are therefore allowable for at least the reasons mentioned above. Withdrawal of the present rejection is respectfully requested.

Conclusion

The foregoing is submitted as a full and complete response to the Official Action. Applicant submits that all remaining claims are in condition for allowance. Reconsideration is requested, and allowance of all remaining claims is earnestly solicited.

Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666. If the Examiner believes that there are any informalities which can be corrected by an Examiner's amendment, a telephone call to the undersigned at (503) 439-8778 is respectfully solicited.

Respectfully submitted,

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